

REMARKS

The Specification and the Abstract have been amended. Proposed changes to Fig. 7 and Fig. 11L have been requested. Claims 1, 6, 15, 17, 29, 36, and 43 have been amended. Claims 48-63 have been cancelled as being directed to a non-elected invention as the Applicants intend to pursue their issuance in a divisional application. Claims 1-47 remain in the application. A marked up version of the changes is found in Appendix A. Further examination and reconsideration of the application, as amended, is hereby requested.

In Appendix B of this Amendment are copies of exhibits used as evidence to support the assertions made herein. The exhibits are supported by declarations under Rule 132 as required by MPEP 716.02.

Exhibit A is a copy a report dated 1/12/2001 disclosing results of the characterization of non-annealed and annealed versions of the emitter.

Exhibit B is a copy of "Thick #1 SiC 50nm EFE051505_009 R6C2 (35um)" dated 2/21/2001 which describes emitter test results of emitters using the invention.

Exhibit C is a copy of further tests after the application was filed which demonstrate the nanohole creation formed by the annealing process disclosed in the application.

Exhibit D is a slide showing the emitter test system used to perform the emission testing.

On Page 2 and Page 4 of the Office Action, the Examiner objected to the drawings under 37 CFR 1.83(a) and 35 USC 112, respectively. In particular, the Examiner stated that the drawings must show every feature of the invention specified in the claims and the Examiner was concerned that the sidewalls were not shown. Applicants respectfully submit that the sidewalls are clearly shown in Fig. 11L and described on page 10, lines 8-13 and would be readily apparent and reasonably convey to one of ordinary skill in the art that Applicants had possession of the claimed invention. However, to further clarify the description, the Applicants are proposing to add reference characters to Fig. 11L and the specification to make the feature of the sidewalls more explicit. No new additional

matter has been added. It should be noted that 37 CFR 1.83(a) only requires that the feature be shown, not that it have a reference character. The specification on page 10, lines 8-13 clearly describes the relationship of the sidewalls as shown in Fig. 11L to the emitter chamber. Removal of this objection is respectfully

5 requested.

On Page 2 of the Office Action, the Examiner objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because reference sign 36 was not mentioned in the specification. Applicants have amended the specification to include the reference designator 36 thereby making the specification consonant with the drawings. Removal of this objection is respectfully requested.

10 On Page 3 of the Office Action, the Examiner objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because the reference sign 54 was not mentioned in the specification. Applicants are submitting herewith a proposed drawing correction to remove reference sign 54 from Fig. 7. Removal of this objection is respectfully requested.

15 On Page 4 of the Office Action, the Examiner stated that the limitation "based-based dielectric layer" in claim 17 had insufficient basis. The Applicants have amended claim 17 to correct this error. The limitation now reads as a "silicon-based dielectric layer." Support for this change is found throughout the specification.

20 The abstract of the disclosure has a grammatical error. Applicants have amended the abstract to correct this error.

25 On Page 3 of the Office Action, the Examiner notes that independent claims 10 and 11 appear to depend from claim 1, that independent claims 23-25 depend from claim 17 and that independent claim 26 depends from claim 25. Applicants are unsure of the Examiner's purpose for this statement but note that this dependent form of claiming is permissible as held by the Board of Patent Appeals and Interferences in in re Moelands, 3 USPQ.2D 1474 (1987).

30 It appears that the Examiner may be using this statement on Page 3 of the Office Action for the purposes of preventing the limitations of a respective parent claim from being considered in the examined dependent claims. If so, Applicants respectfully disagree with this interpretation of MPEP 608.01 (n). Applicants

assert that rather than being *independent* claims, claims 10, 11 and 23-26 are proper *dependent* claims that comply with 35 USC 112, 4th paragraph. Each constitute “a further limitation of the subject matter claimed,” are not broader than their parent claims. In addition, no element of any respective parent claim is
5 deleted or replaced by any other element in claims 10, 11, and 23-26. These claims incorporate by reference all the limitations of the claim to which each refers as required by 35 USC 112, 4th paragraph. Furthermore, a product which would infringe an integrated circuit of claim 10, the electronic devices of claims 11 and 25, the display device of claim 23, the storage device of claim 24, or the computer
10 system of claim 26 would also infringe the respective parent claim. The Board in in re Moelands noted that they read MPEP §608.01(n) (Dec. 1985) as being consistent with their decision. Accordingly, the Applicants believe the Examiner has made an error in not considering the limitations of the respective parent claim in the examination of claims 10-11, and 23-26 and requests reexamination and
15 reconsideration of these claims in addition to the additional representations of patentability discussed below.

In particular for claims 10 and 23, the Examiner on Page 4 of the Office Action rejected claims 10 and 23 under 35 USC 102(b) as being anticipated by
20 Nakatani et al. As noted in MPEP 2131, “a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” As noted above, claim 10 includes the limitation “the emitter of claim 1 disposed on the substrate” and therefore incorporates the limitations of claim 1 which includes the limitation of “a silicon-
25 based dielectric layer disposed on the electron supply.” Nakatani is directed to a flat display the uses field emission tip emitters that are “conical metal elements each having a sharp tip formed of a metal” (See col. 5, 59-64). Nowhere in Nakatani can the Applicants find “a silicon-based dielectric layer disposed on the electron supply” that Applicants are claiming. Indeed, the operation of a field
30 emission tip emitter does not require the presence of a “silicon-based dielectric layer” used as a tunneling layer for electrons as field tip emitters use high electric field strength only and not electron tunneling under high electric fields for emission. Accordingly, Nakatani does not disclose, teach, or suggest Applicants’ claimed invention.

In addition, the Examiner asserts that Nakatani discloses “circuitry for operating the emitter.” Applicants respectfully traverse this statement of the Examiner. As noted in the disclosure of Nakatani, “the emitter electrode lines serve as a power supply line to apply a negative voltage (e.g. -40V)” and the “gate electrode lines serve to supply a voltage (e.g. 40V for extracting electrons from the emitter tips” (see col. 5, lines 66-67 and col. 6, lines 11-12). Rather than providing for “circuitry for operating the emitter formed on the substrate with the emitter” as Applicants are claiming, Nakatani merely provides for power and control lines for accessing the emitters as is traditionally done with conventional displays. Indeed, the -40V and 40V differential voltage (80V total) applied to the emitter rules out using conventional control circuitry from being “formed on the substrate with the emitter” as Applicants are claiming. As noted in Applicants’ disclosure on page 4, lines 28-30, the emitter of Applicants’ claimed invention only requires about 3-10V to operate which is within the range of conventional control circuitry in integrated circuits. One aspect of Applicants’ invention provides that the operating voltage that enables the emitter to emit is lowered substantially from prior art voltage levels thus allowing for the “circuitry for operating the emitter” to be “formed on the substrate with the emitter.” Accordingly, Nakatani alone or in combination does not anticipate or suggest Applicants’ claimed invention.

In particular for claim 23, the Examiner stated that Nakatani discloses “an integrated circuit including the emitter (3a) wherein the emitter emits a visible light source.” Applicants respectfully traverse the Examiner’s assertion for several reasons:

First, as noted above, claim 23 depends on claim 17 and thus incorporates the limitations of claim 17. Claim 17, as amended, includes the limitation of where the emitter includes “a silicon-based dielectric layer formed on the electron supply layer in the opening.” As noted for claim 10, Nakatani does not disclose, teach or suggest a silicon-based dielectric layer as Nakatani only discloses using a field emission tip emitter which is a different type of emitter than Applicants’ silicon-based dielectric tunneling emitter.

Second, Nakatani does not disclose the limitation of “wherein the *emitter* creates a visible light source” as Applicants are claiming. Indeed, as shown in Fig. 2 of Nakatani, the emitter tips 1 only emit electrons that impinge fluorescent layer 8, which then creates photons that are directed back past the emitter tips 1

to a watching eye (see col. 9, lines 29-41). Accordingly, Nakatani does not disclose, teach, or suggest that "the *emitter creates* a visible light source" but rather that the emitter emits electrons which "impinge upon the fluorescent layers 8 from which excitation light is emitted." The fluorescent layers 8 do not form a
5 part of the emitter.

Third and finally, the Examiner asserts that Nakatani discloses "a lens (8) for focusing the visible light source, wherein the lens is coated with a transparent conducting surface to capture electrons". As noted previously, reference 8 is directed to a fluorescent layer and not a "lens for focusing" as Applicants are
10 claiming. Nor does the fluorescent layer 8 include a "transparent conducting surface to capture electrons." Indeed, the fluorescent layer 8 would not be operational if it included a transparent conducting surface that captured the electrons before they were to impinge on the fluorescent layer as it is the electrons striking the fluorescent layer that causes the fluorescent layer to
15 electroluminesce and from which excitation light is emitted.

Accordingly, Nakatani does not alone or in combination with the prior art made of record disclose, teach or suggest Applicants' claimed invention for claims 10 and 23 and removal of the rejection under 35 USC 102(b) is respectfully
20 requested.

On Page 4 of the Office Action, the Examiner rejected claims 11, 13, 14, and 25-28 under 35 USC 102(b) as being anticipated by Xia. As noted previously, claims 11, 13, and 14 depend directly or indirectly on independent claim 1 and thus incorporate the limitations of claim 1. Similarly, claims 25-28 depend directly
25 or indirectly on independent claim 17 and thus include all the limitations of claim 17. Xia is directed to a "Single Pixel Tester for Field Emission Displays" (See title, abstract and col. 3, lines 55-67.) Xia does not disclose, teach, or suggest the limitation of a "silicon-based dielectric layer" nor that "the emitter has been subjected to an annealing process to create nano-porous openings in the cathode
30 layer" as Applicants are claiming in claims 1 and 17, as amended, and which is included by way of dependent limitation in claims 13, 14 and 25-28. Accordingly, because "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," Xia does not anticipate claims 11, 13, 14, and 25-28. In addition, as

will be discussed below, Applicants believe independent claims 1 and 17, as amended, to be patentable over the art made of record. Accordingly, dependent claims 11, 13, 14 and 25-28 are believed patentable based on the patentability of their respective independent claims.

5 Claim 25 includes the additional limitation of a “focusing device for converging the emissions from the emitter.” This limitation is not disclosed, taught or suggested by Xia. At most, Xia discloses an extraction gate or grid structure 15 (Fig. 1 and col. 1, lines 36-37). This extraction grid collects stray electrons but is not used as “a focusing device for converging the emission from the emitter” as
10 Applicants are claiming. Claims 26-28 depend directly or indirectly on claim 25 and are deemed patentable based at least on the patentability of parent claim 25.

 Accordingly, for the foregoing reasons, Xia does not anticipate claims 11, 13, 14 and 25-28 and removal of the rejection under 35 USC 102(b) is respectfully
15 requested.

 On page 5 of the Office Action, the Examiner rejected claim 29 under 35 USC 102(b) as being anticipated by Gibson et al. The Applicants believe the Examiner meant to reject claim 24 as it is directed to a storage device similar to Gibson et al and matches the content of the Examiner’s rejection. It should be
20 noted for the record that Gibson is commonly assigned to the same assignee as the instant application, i.e. Hewlett-Packard Co. Dependent claim 24 depends directly on independent claim 17, as amended, and as earlier discussed includes all the limitations of its parent claim. Accordingly, the storage device of claim 24 includes an “integrated circuit” that includes the emitter of claim 17, as amended,
25 which has the limitations of a “silicon-based dielectric layer” and “wherein the emitter has been subjected to an annealing process to create nano-porous openings in the cathode layer.” These limitations are not disclosed, taught or suggested by Gibson as Gibson discloses “*field* emitters ... the type that can produce electron beams that are *narrow enough* to achieve the bit density of the storage medium, and *can provide the power density* of the beam current needed
30 for reading and writing to the medium” (see col. 3, lines 39-44). Therefore, Gibson discloses the use of “field emitters” and not a tunneling emitter with a “silicon-based dielectric layer” “subjected to an annealing process” as Applicants are claiming. Nor would it be obvious to substitute a tunneling emitter (also known as

a flat (vs. tip) emitter) for the field emitter. In Gibson's application, the emitter must be capable of producing a narrow beam at a sufficient power density to read and write the medium. Conventional tunneling emitters are unable to meet this requirement while Applicants' disclosed and claimed emitters provide a power
5 density 10-1000x (as discussed below) more than that found with prior art tunneling emitters. Thus, Applicants' annealed tunneling emitters are now comparable in power density of field emitters and allows for operation of the emitter in less stringent vacuum environments thus allowing for higher reliability, lower costs, and less complex packaging. Accordingly, Gibson does not
10 anticipate nor suggest Applicants' claimed invention. Removal of the rejection under 35 USC 102(b) for claim 24 is respectfully requested.

On Page 6 of the Office Action, the Examiner rejected claims 1-10 under 35 USC 103(a) as being unpatentable over Chuman. The Examiner stated that
15 Chuman discloses all the limitations of claim 1 including the electron supply, a molybdenum cathode layer, and a 500 Angstroms thick SiNx dielectric layer. In regard to the limitation of "wherein the electron supply, silicon-based dielectric layer, and cathode layer have been subjected to an annealing process;" the Examiner states that this limitation makes claim 1 a product by process claim.
20 The Examiner then notes that the Applicant has the burden of proof in such cases as the case law makes clear.

In in re Spada, 911 F.2d 705, 709, 15 USPQ.2D 1655 (Fed. Cir. 1990), the Federal Circuit concluded that the Board of Patent Appeals (PTO) was correct in requiring that an Applicant in a product-by-process claim, upon sound basis that
25 the prima facie case has been made, to have the burden of proof *to show they are not the same structure*. The PTO suggested, and the Federal Circuit agreed, that an Applicant should provide some scientific explanation for the asserted differences between the properties of his compositions and those described by the prior art. The court went on to say that "[w]hile an inventor is not required to
30 understand how or why an invention works, we think that the PTO was correct, in view of the apparent identity of the compositions, in requiring Spada to distinguish his compositions from those of [the prior art]." The court implied that the evidence must relate to the fundamental question of novelty of the claimed invention over the prior art otherwise evidence of unobviousness is superfluous. *Id.* In Spada,

the court stated that the Applicant is *reasonably* required to show that his claimed composition is different from those describe by the prior art.

While it is well established that an Applicant for patent need not understand the theory of operation of his invention (Eames v. Andrews, 122 U.S. 40 (1887)),

5 it appears that the Applicants are required to do so to overcome the shift in the burden of persuasion. Accordingly, Applicants have further investigated the remarkable results of their invention and how can further describe the physical changes and possible theory of operation as to why their process produces a emitter that is physically different in both the kind of structure and the degree of
10 results obtained. Applicants believe that they have clearly shown in the disclosure how to achieve the claimed results even though at the time of filing they did not understand of the difference in structure and theory of operation for the unexpected properties. However, Applicants did detail the unexpected properties. For instance, on page 10, lines 17-18, the Applicants state that the emitter is
15 subjected to an annealing process to increase the amount of electron emission from the emitter. Figs. 12A and 12B are shown and described as two exemplary annealing processes. Other effects of the annealing process include increased device yields and increased operating lifetime. Noticeable physical differences include decreased resistance of the contacts of dissimilar metals which increases
20 the current flow to the emitters.

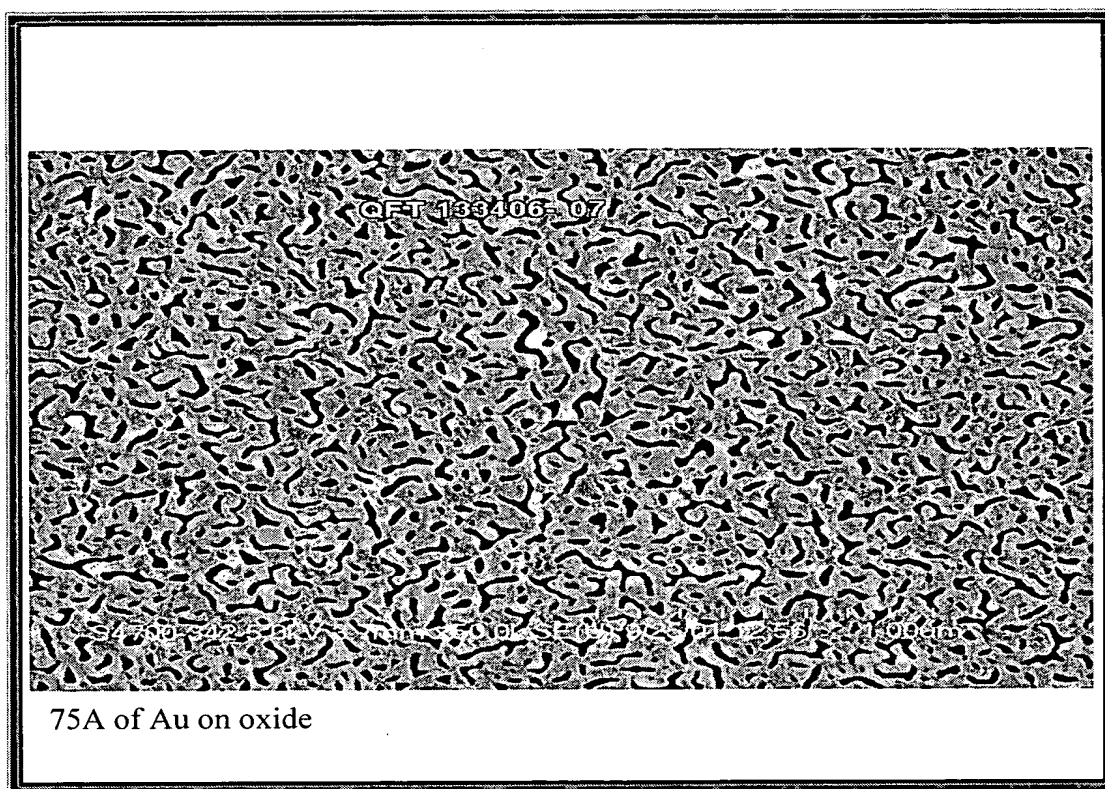
Since filing of the application, the inventors have performed additional tests to better understand the theory of operation and the physical differences from that of the prior art. Among the differences are that:

1) The contact resistance decreases at the interface between the tunneling
25 layer and the electron source, and at the interface between the tunneling layer and the cathode layer. This effect is typical of metal interfaces that are subjected to annealing and would likely be expected.

2) *Most importantly*, the top structure of the cathode layer is transformed during the annealing process to create *nano-sized porous pinholes* or openings.

30 These openings allow the electrons that tunnel across the energy barrier to escape without losing momentum due to collisions in the cathode layer. If the cathode layer does not have openings, then the electrons that tunnel must have sufficient momentum (energy) remaining after the tunneling to escape through the thin layer of cathode material. By having openings, electrons that tunnel that have

less than sufficient energy to escape the cathode layer previously can now exit through the openings. This greatly increases the number of electrons that can be emitted from the tunneling emitter. These openings also allow for photon emission because without the openings, the photons would ordinarily be absorbed
5 into the opaque cathode layer. By allowing a wide range of tunneled electron energies to escape through the openings, the nanoholes in the cathode layer help to reduce spiking in the emission output and improves the emission stability. Below is a Figure from Exhibit C which exhibits the nano hole structure in a 75 Angstrom gold cathode layer.

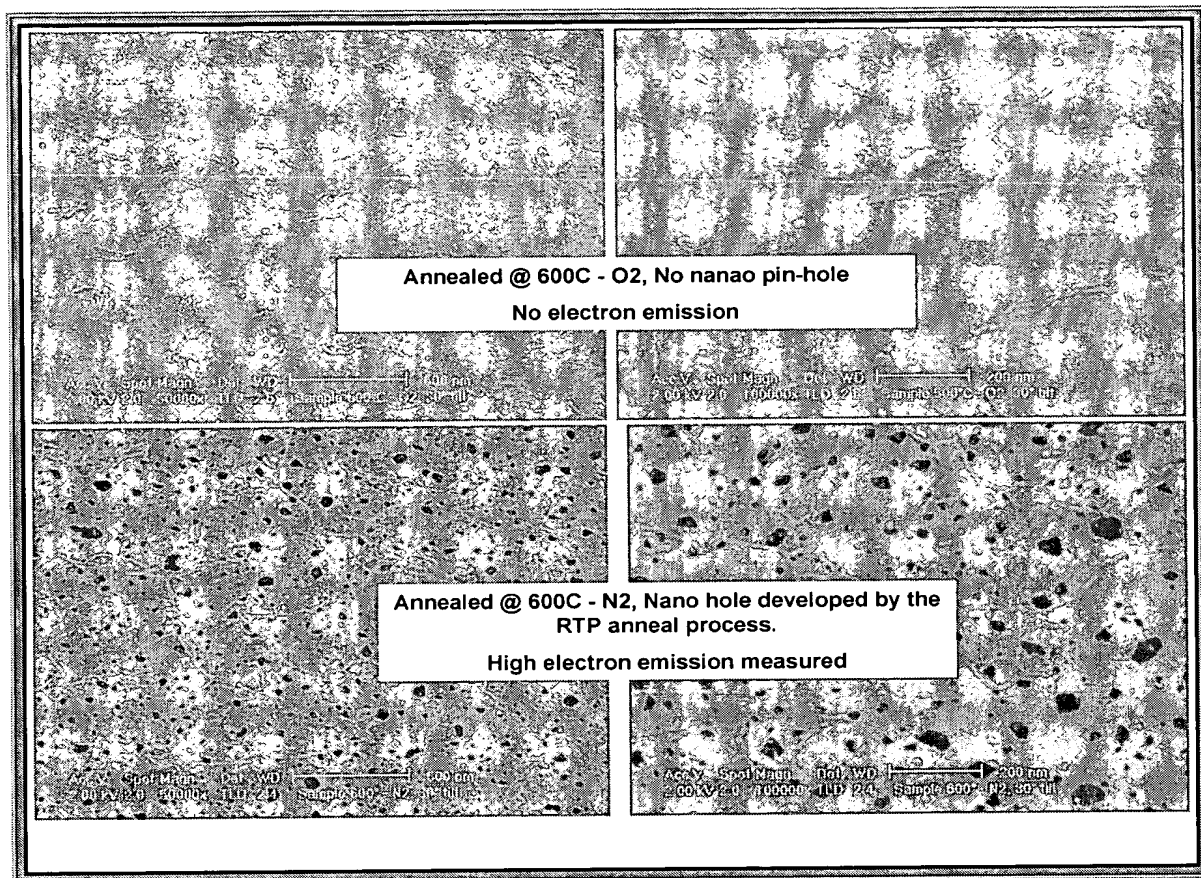


Portion of Exhibit C – Electron Microscope Picture of
Nanohole Structure in Gold Cathode Layer

Subsequent tests (see Exhibit C) have shown that when the emitter is annealed in an only oxygen or only argon environment the nano-holes are not
15 formed. However, nanoholes are formed when annealing is performed with either an air (which contains 78% nitrogen, 21% oxygen) or a nitrogen only atmosphere. Thus, it appears that tunneling layer undergoes a transformation during annealing by introducing impurities of nitrogen into the tunneling layer. Furthermore, the

cathode layer is physically changed during annealing to create a layer with nano-sized holes that allow for increased electron and photon emissions.

Below is a Figure from Exhibit C which demonstrates the results of annealing a ~70 Angstrom platinum cathode layer in O₂ in which nanoholes were not formed and annealing a ~70 Angstrom platinum cathode layer in N₂ in which the nanoholes were formed.



Portion of Exhibit C – Effect of Nitrogen on Nanohole Creation

It is evident that these differences in physical properties due to annealing the emitter lead to a novel structure different from that described in the prior art. As evidence of the novel structure, the change of the emitter due to annealing produces unexpected results in the form of increased emissions, photonic emissions, and more stable emissions which make the claimed invention unobvious over the prior art. Further evidence is the electron microscope pictures showing the nanohole formation that alters the structure of the cathode layer.

Determining whether the results are truly unexpected is addressed in the MPEP in §716.02. According to MPEP 716.02, a greater than expected result is

an evidentiary factor pertinent to the legal conclusion of obviousness. Evidence of a greater than expected result may be shown by demonstrating an effect which is greater than the sum of each of the effects taken separately. The evidence should establish that the differences in result are in fact unexpected and

unobvious and of both statistical and practical significance.

Following are exemplary test results from the chart in Exhibit B for an emitter with a Silicon Carbon (SiC) tunneling layer of 500 angstroms thickness and a 35 micron diameter emitter surface

:~ 120 nA peak emission, average emission of 5nA.

The current density of the emitter can be calculated based on the emitter size and the emission current. The emitter size reported is the diameter of the emitter in microns. The emission current reported (I_e) is in units of nanoamperes.

Thus the current density in terms of Amps/cm² is:

$$\text{Current density in Amps/cm}^2 = I_e \text{ Amps} / (10000 \text{ cm}^2/\text{m}^2 * 3.14 * (1/2 * \text{emitter size in meters})^2)$$

For the 35um SiC with 120nA, this emitter has a current density of:

$$120\text{E-9 Amps} / (10000 * 3.14 * (1/2 * 35\text{E-6})^2) = 0.012 \text{ Amps/cm}^2$$

During typical operation, these emitters will be pulsed with extremely small duty cycles, thus allowing for increased emissions due to less localized heating. By having less localized heating, the leakage current is reduced and there is less vibrations in the materials of the tunneling and cathode layers. These lower vibrations will allow more electrons to escape rather than be deflected or adsorbed. It is expected that emission currents from this low duty-cycle pulsed operation will be substantially higher, such as two to four times that measured. Therefore, these results support the claimed ranges of Applicants invention of providing an emission current of at least 10 mAmps/cm² which is an order of magnitude greater than that accomplished by the prior art devices (which report up to 1mAmps/cm²). These are truly unexpected results of both statistical and practical significance (see MPEP 716.02(b)), principally created by the nanohole

structure in the cathode layer and lowering of the tunneling resistance created by the annealing process. Both the emission results and the structural changes to the emitter due to the annealing process are evidence of unexpected results and evidence of non-obviousness over the prior art. As noted by MPEP 716.02(d), the
5 “objective evidence of nonobviousness must be commensurate in scope with the claims which the evidence is offered to support.”

Applicants believe that they have demonstrated the non-obviousness of the claimed emitter and that the subjecting the claimed emitter to an annealing
10 process creates both statistically and practical significant results which were previously unknown to those skilled in the art and therefore not disclosed, taught, or suggested by the art made of record. Thus, Applicants have reasonably shown that the claimed combination is different from that of the prior art. This argument and evidence should be sufficient to overcome the shift in the burden of
15 persuasion due to the Examiner’s assertion of the “product by process” argument.

Further, the Applicants have demonstrated that the physical structure of the product by process emitter is indeed different from that of the cited art and that the physical structure is an inherent property of the emitter after it has been subjected to the annealing process. Accordingly, the Applicants are amending the
20 independent claims to include this physical structure that is an inherent property and adding support in the specification. By adding the additional structure, it is believed that the Examiner’s “product by process” assertion has been obviated. The Applicants believe that based on case law and the MPEP that no new matter has been entered.

As noted in MPEP 2163.07(a), “by disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The Application may be later amended to recite the function, theory or advantage
25 without introducing prohibited new matter.” Support for this position is found in In re Nathan, 328 F.2d 1005, 140 USPQ 601 (CCPA 1964) and Kennecott v. Kyocera, 835 F.2d 1419, 5 USPQ.2D 1194 (Fed. Cir. 1987). In in re Nathan, the court held that an amendment to the specification which clarified the structure of the invention based on extraneous evidence discovered after the filing of the
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application is permissible if their original disclosure sufficiently identified the claimed subject matter in terms of measured physical properties. (328 F.2d at 1008.) In Kennecott, the court held that since “anyone with a microscope would see the microstructure of the product”, the “disclosure in a subsequent patent application of an inherent property of a product does not deprive that product of the benefit of an earlier filing date.” (835 F.2d at 1423.) Accordingly, the Applicants have amended the specification to add the recitation of the advantage of the nano-porous openings. The paragraph starting on page 10, line 19 has been amended to include the sentence: “Examination of the annealed emitters reveals that the cathode layer has nano-porous opening on the order of less than 200 nanometers in at least one direction of length, width, or diameter.” This advantage of the nano-porous openings would be readily visible to one of ordinary skill in the art when viewing the annealed emitter with an electron microscope. Therefore the nano-porous openings are an inherent property and thus no new matter has been added to the specification. Accordingly allowance of claim 1, as amended, is respectfully requested. Dependent claims 2-10 depend directly on claim 1 and are believe patentable based at least on the patentability of claim 1.

Further, there are additional limitations which impart patentability to these dependent claims, some of which will now be discussed. The Examiner states that Chuman discloses an emission device that has an emission current greater than 1×10^{-3} Amps/cm² and that it would be obvious . . . to modify Chuman to include an emission current greater than 1×10^{-3} Amps/cm² because it aids in providing high luminance. Applicants respectfully traverse the Examiner’s assertion of obviousness. The Examiner has failed to state how to modify Chuman’s emitter to get higher density or how Chuman itself discloses, teaches, or suggest a higher current density than 1mA/cm². Thus, the Examiner’s assertion is a mere conclusion without factual evidence or reason

As discussed previously, the claimed emission is expressed in terms of current density per area. It would not be obvious to increase the emissions of Chuman, as one could not increase the current density per area by simply making the emitter larger. The Applicants have increased the emission current density by subjecting the emitter to an annealing process that changes the structure of the emitter by creating nano-porous openings, thus allowing for higher emissions. Indeed, Chuman shows in its Fig. 2a a maximum current density output of about 1

x 10^{-3} Amps/cm² by manipulating *the tunneling layer thickness*. The Applicants have been able to far exceed this disclosed current density by at least one order of magnitude (a factor of 10X). In making the combination obvious, the Examiner does not disclose how one skilled in the art would increase the current density nor
5 does Chuman disclose, teach, or suggest a current density greater than 1×10^{-3} Amps/cm². If the Examiner continues to assert this rejection, the Applicants respectfully request the Examiner to provide an affidavit describing how to do so or to supply a reference that teaches Applicants' structure, as amended.

In contrast, the Applicants have disclosed and claimed how to increase the
10 current density by using an annealing process and its ability to respectively alter the structure of the emitter by lowering the tunneling layer resistance, reducing ohmic contacts, and most importantly, creating nano-porous openings in the cathode layer. It is through the application of the annealing process that these unexpected results have been obtained. None of these changes in structure have
15 been disclosed, taught, or suggested by the proposed combination or other art made of record. Further evidence of the state of the art in electron emission density is found in Kusunoki on page 1667 (bottom of left column) wherein the emission current to date (8/20/99 when manuscript received) is 50×10^{-6} Amps/cm². The desire for at least 1 mA/cm² is noted. In Fig. 5, Kusunoki only
20 discloses an emission density of up to this 1mA/cm² limit, i.e. the same as Chuman. Accordingly, the rejection under 35 USC 103(a) and allowance for claims 2-10 are respectfully requested.

On Page 7 of the Office Action, the Examiner rejected claim 12 under 35
25 USC 103(a) as being unpatentable over Xia in view of Gibson. In particular, the Examiner states that Xia discloses an emission display with a reading circuit and discloses all other limitations except for the electronic device to be a mass storage and the anode to be a recording medium. The Examiner states that Gibson discloses a storage device and an anode storage area. Therefore,
30 according to the Examiner it would be obvious to modify the display of Xia to incorporate a mass storage device and recording media to provide storage data as taught by Gibson. Applicants respectfully traverse this rejection for several reasons. First, Xia is directed to a single pixel tester for "field emission displays" and thus does not even remotely suggest let alone teach or disclose its use as a

storage device. Second, Xia discloses a “field emission tip emitter,” the same type of emitter as that disclosed in Gibson. Claim 1, as amended, upon which claim 12 indirectly depends, is claiming a “tunneling emitter” with “a silicon based dielectric layer disposed” on an “electron supply” and a “cathode layer disposed
5 on the silicon based dielectric layer” that has been subjected to an “annealing process” to “create nano-porous opening in the cathode layer.” These limitations are not disclosed, taught, or suggested by Xia or Gibson alone or in combination. Accordingly, removal of the rejection and allowance of claim 12 is respectfully requested.

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On Page 7 of the Office Action, the Examiner rejected claims 15, and 16 under 103(a) as being unpatentable over Chuman in view of Gibson. Claim 15 has been amended to include the limitation wherein the emitter includes “a cathode layer disposed on the silicon-based dielectric layer” and that the emitter
15 has been subjected to an annealing process “to create nano-porous openings in the cathode layer.” The Applicant has explained previously for claim 1 why the annealing process provides unexpected and non-obvious results thereby indicating that the structure of the emitter is different than that of the prior art. However, the Applicants have amended the claim to include the limitation of nano-
20 porous openings that are created by the annealing process to provide additional structural limitation thereby obviating the product by process argument asserted by the Examiner. These limitations are not disclosed, taught, or suggested by Chuman or Gibson alone or in combination. Accordingly, removal of the rejection under 35 USC 103(a) and allowance of claims 15 and 16 are respectfully
25 requested.

On Page 9 of the Office Action, the Examiner rejected claims 17-22 under 35 USC 103(a) as being unpatentable over Chuman in view of Moyer. Applicants have amended claim 17 to include the limitation of where the emitter has been
30 subjected to an annealing process “to create nano-porous openings in the cathode layer.” As discussed previously with respect to claim 1, this limitation is not disclosed, taught, or suggested by Chuman or Moyer alone or in combination.

Further with respect to claims 19, the Examiner states that it would have been obvious to modify Chuman to achieve an emission rate of 0.01 Amps/cm².

However, this is just a conclusionary statement without any reasoning or basis to support it. Chuman only discloses being able to achieve a $0.001\text{Amp}/\text{cm}^2$ emitter by varying the dielectric thickness. Since the current density is expressed in terms of current per surface area, merely making the emitter bigger does not
5 increase the current density. Applicants are able to increase the current density by using the annealing process to create the nano-porous openings which allow tunneled electrons to pass through the cathode layer without losing momentum. Accordingly, claim 19 is believed separately patentable over Chuman and Moyer.

Claims 18, 20, 21 and 22 depend directly on claim 17 and are believed at
10 least patentable based on the patentability of claim 17.

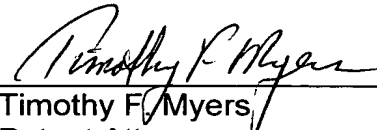
Removal of the rejection under 35 USC 103(a) and allowance for claims 17-22 are respectfully requested.

On Page 10 of the Office Action, the Examiner rejected claims 29-35 and
15 43-47 under 35 USC 103(a) as being unpatentable over Chuman and Moyer and Huang. Applicants have amended claim 29 and claim 43 to include the limitation of the cathode layer having "nano-porous openings" similar to that describe above for claims 1 and 17. Applicants believe this additional structural limitation obviates the "product-by-process" assertion made by the Examiner. Claims 30-35 depend
20 on claim 29 and are believed patentable at least on the patentability of claim 29. Claims 44-47 depend on 43 and are believed patentable at least on the patentability of claim 43.

Applicants believe their claims as amended are patentable over the art of record, and that the amendments made herein are within the scope of a search properly conducted under the provisions of MPEP 904.02. Accordingly, claims 1-47 are deemed to be in condition for allowance, and such allowance is respectfully requested.

Respectfully Submitted,

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APPENDIX A
Marked-up Version of Changes

In the Specification:

5

Please replace the paragraph on page 5 lines 13-25 with the following:

Fig. 2 is an exemplary diagram of a use for the emitter 50 of Fig. 1. In this application, the electron emission 16 is focused by an electrostatic focusing
10 device or lens 28, exemplified as an aperture in a conductor that is set at predetermined voltage 36 that can be adjusted to change the focusing effect of the lens 28. Those skilled in the art will appreciate that lens 28 can be made from more than one conductor layer to create a desired focusing effect. The electron emission 16 is focused by lens 28 into a focused beam 32 onto an anode
15 structure 30. The anode structure 30 is set at an anode voltage V_a 26 which magnitude varies for an application depending on the intended use and the distance from the anode structure 30 to the emitter 50. For instance, with anode structure 30 being a recordable medium for a storage device, V_a might be chosen to be between 500 and 1000 Volts. The lens 28 focuses the electron emission 16
20 by forming an electric field 34 within its aperture. By being set at a proper voltage from V_e , the electrons emitted from the emitter 50 are directed to the center of the aperture and then further attracted to the anode structure 30 to form the focused beam 32.

25 Please replace the two paragraphs beginning on Page 10, line 3 with the following:

Fig. 11K illustrates the application of a cathode photoresist layer 116 that has been applied and patterned to define openings where the cathode layer 14 is
30 to be etched to isolate multiple emitters on the substrate 10. Fig. 11L illustrates the cathode layer 14 after it has been etched and the cathode photoresist 116 removed. Within the emitter chamber 114 is the emitter surface 86. An exemplary top view of the resulting structure is shown in Fig. 8. The emitter surface 86 has a first area. The emitter chamber 114 has a first chamber section

interfacing to the emitter surface 86 that has substantially parallel sidewalls 81 within the adhesion layer 80. The emitter chamber 114 has a second chamber section formed in the conductive layer 82 that has sidewalls 83 that diverge to an opening having a second area. The second area is larger than the first area. The cathode layer 14 is disposed on the emitter surface 86 and the sidewalls (81,83) of the first and second sections of the emitter chamber 114. By using integrated circuit thin film technology to fabricate the emitter, it can be integrated along with traditional active circuits found on conventional integrated circuits. The integrated circuit with the emitter can be used in display devices or storage devices as previously described. Preferably, after fabrication, the emitter is subjected to an annealing process to increase the amount of emission from the emitter.

Fig. 12A and 12B are charts of exemplary annealing processes which are used to increase the emission current capability of an emitter embodying the invention. The annealing process also increases the device yields and quality by allowing the emitters to last longer. The annealing process, among other benefits, helps to decrease the resistance of contacts of dissimilar metals thereby increasing the current flow to the emitters. Examination of the annealed emitters reveals that the cathode layer has nano-porous opening on the order of less than 200 nanometers in at least one direction of length, width, or diameter.

In the Abstract:

An emitter has an electron supply layer and a silicon-based dielectric layer formed on the electron supply layer. The silicon-based dielectric layer is preferably less than about 500 Angstroms. Optionally, an insulator layer is formed on the electron supply layer and has openings defined within [in]which the silicon-based dielectric layer is formed. A cathode layer is formed on the silicon-based dielectric layer to provide a surface for energy emissions of electrons and/or photons. Preferably, the emitter is subjected to an annealing process thereby increasing the supply of electrons tunneled from the electron supply layer to the cathode layer.

In the Claims:

1. (Amended) A[n] tunneling emitter, comprising:

an electron supply;

a silicon-based dielectric layer disposed on the electron supply; and

a cathode layer disposed on the silicon-based dielectric layer;

wherein the electron supply, silicon-based dielectric layer, and cathode layer have been subjected to an annealing process to create nano-porous openings in the cathode layer.

MM

6. (Amended) The emitter of claim 1 operable to provide an emission current of greater than 1×10^0 Amps per square centimeter.

15. (Amended) A storage device, comprising:

at least one emitter to generate an electron beam, the emitter having a silicon-based dielectric layer having a thickness between about 250 to 5000 Angstroms, and a cathode layer disposed on the silicon-based dielectric layer, the at least one emitter subjected to an annealing process to create nano-porous openings in the cathode layer;

a lens for focusing the electron beam to create a focused beam; and
a storage medium in close proximity to the at least one emitter, the storage medium having a storage area being in one of a plurality of states to represent the information stored in that storage area;

such that:

an effect is generated when the focused beam bombards the storage area;
the magnitude of the effect depends on the state of the storage area;
and

the information stored in the storage area is read by measuring the magnitude of the effect.

17. (Amended) An emitter, comprising:

an electron supply layer;

an insulator layer formed on the electron supply layer and having an opening defined within;

5 a silicon-based dielectric layer formed on the electron supply layer in the opening and further disposed over the insulator layer; and

a cathode layer formed on the silicon-based dielectric layer;

wherein the emitter has been subjected to an annealing process to create nano-porous openings in the cathode layer and to increase the supply of electrons
10 tunneled from the electron supply layer to the cathode layer for energy emission.

29. (Amended) An emitter, comprising:

an electron supply surface;

an insulator layer formed on the electron supply surface and having a first opening defined within;
15

a silicon-based dielectric layer formed on the electron supply layer within the first, opening and further disposed on the insulator layer;

an adhesion layer disposed on the silicon-based dielectric layer, the adhesion layer defining a second opening aligned with the first opening;

20 a conductive layer disposed on adhesion layer and defining a third opening aligned with the first and second openings; and

a cathode layer disposed on the silicon-based dielectric layer and portions of the conductive layer, wherein the portion of the cathode layer on the silicon-based dielectric layer is an electron-emitting surface having nano-porous openings.
25

36. (Amended) An emitter, comprising:

an emitting surface having a first area and nano-porous openings;

a first chamber having substantially parallel sidewalls interfacing to the emitting surface; and
30

a second chamber interfacing to the first chamber and having sidewalls diverging to an opening having a second area larger than the first area.

43. (Amended) An integrated circuit, comprising:

a conductive surface to provide an electron supply;

at least one emitter formed on the electron supply including,

an insulator layer having at least one opening to define the location

5 and shape of the at least one flat emitter device,

a silicon-based dielectric layer disposed within the at least one opening of the insulator layer and further disposed over the insulator layer;

a conductive layer disposed over the silicon-based dielectric layer,

the conductive layer having at least one opening in alignment with the at

10 least one opening; and

a cathode layer disposed over the silicon-based dielectric layer and partially over the conductive layer, the cathode layer having nano-porous openings.

Appendix B

Exhibits

5 Exhibit A – “Direct Tunneling Emitter Process Development and Improvement,”
dated 1/12/2001. This status report describes the differences observed between
annealed and unannealed emitters.

Exhibit B - “Thick #1 SiC 50nm EFE051505_009 R6C2 (35um),” dated 2/21/2001
This test report describes emitter test results of emitters using the invention.

10

Exhibit C – “Nano Holes in Thin Metal Layer – A Key for the Electron Emission for
Flat Emitter Device,” undated. This slide presentation shows the changes in the
cathode layer due to the affects of annealing the emitters.

15 Exhibit D – “Emitter Energy Testing,” undated. This slide shows the test setup
used to measure the diode and emission currents to better understand how the
results listed in Exhibit B were obtained.

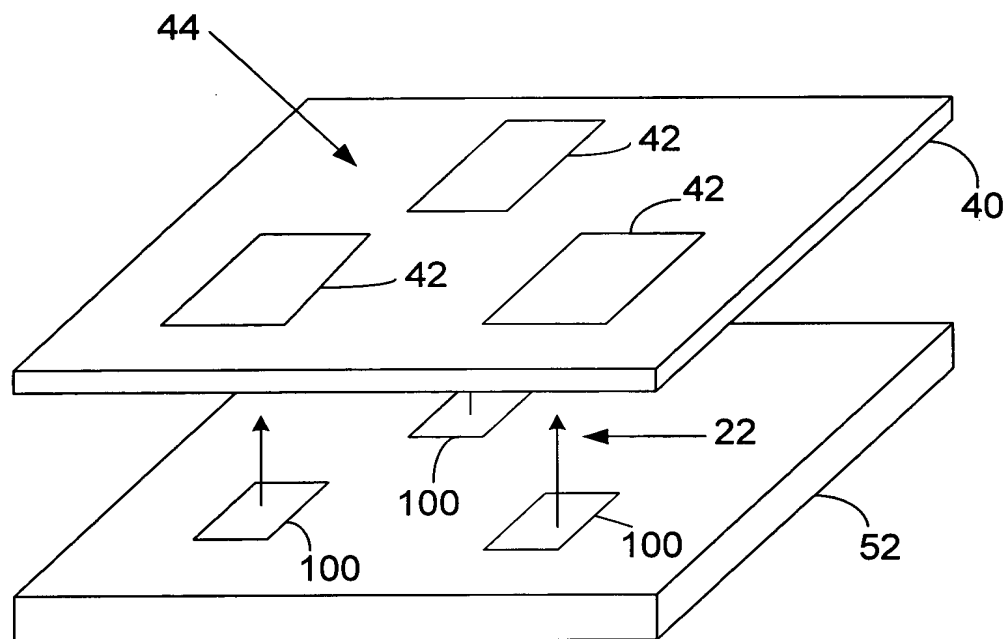


Fig. 7

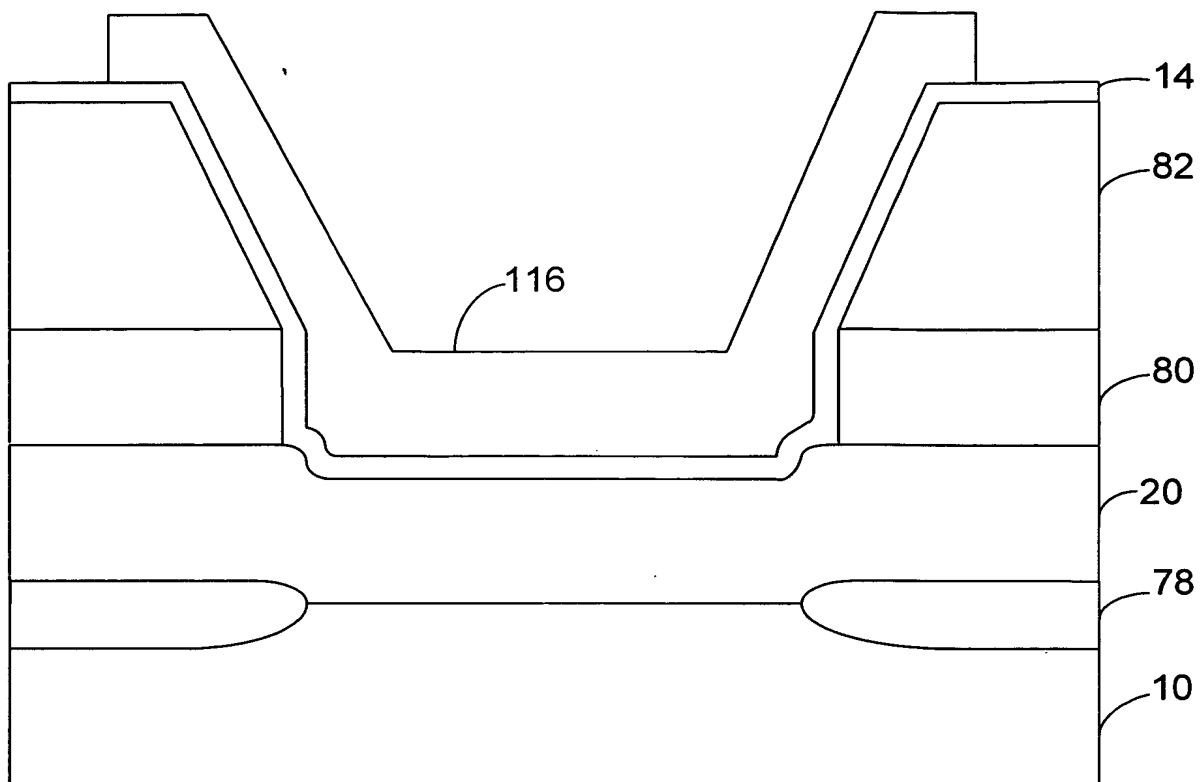


Fig. 11K

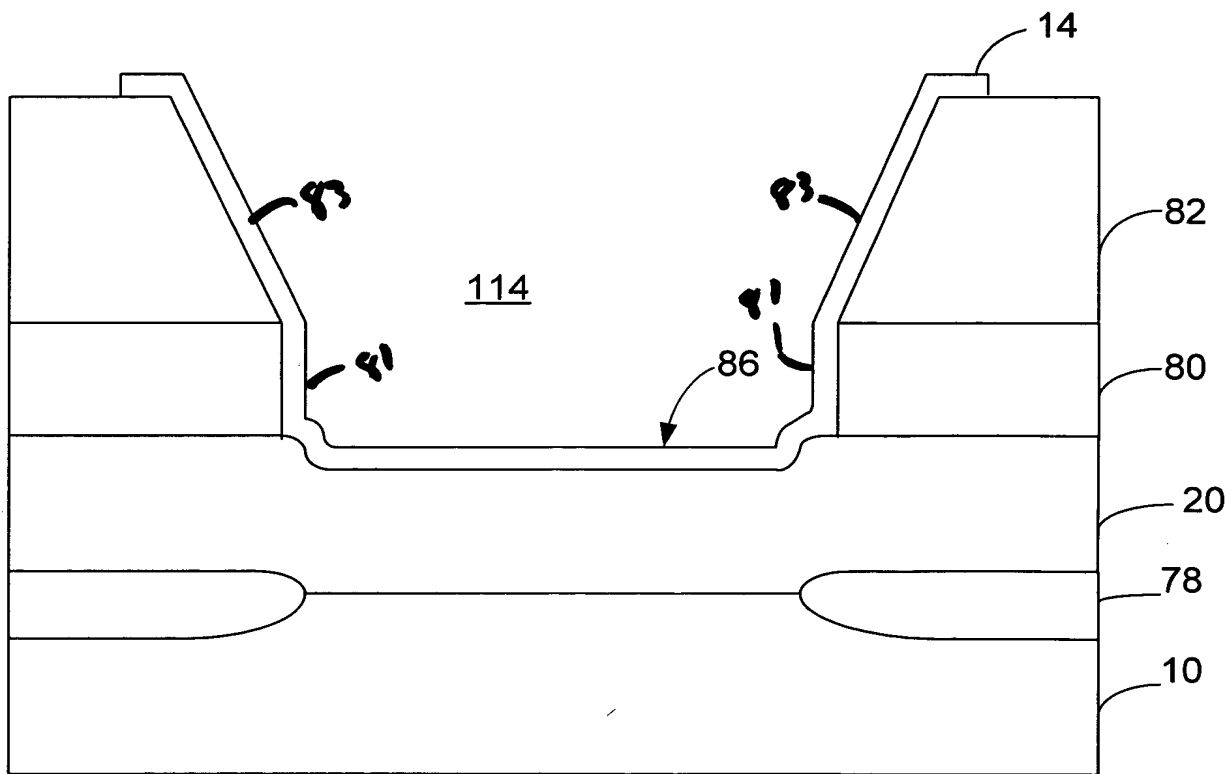


Fig. 11L



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Handwritten: #8
Hewlett
12/23/02

In re application of: Chen, Zhizhgang, et al. Art Unit: 2822
Serial Number: 09/846,047 Examiner: Rose, Kiesha
Filed: April 30, 2001
Attorney Docket: 10007763-1
Title: SILICON-BASED DIELECTRIC TUNNELLING EMITTER
Date: November 19, 2002

DECLARATION UNDER RULE 132

I, Zhizhang Chen, do hereby declare and say:

My home address is 4411 Snowbrush Dr., Corvallis, Oregon.

I have a BS and MS in Electronics from Nankai University, Tianjin, China, a MS in physics from Oregon State University and a Ph.D in Material Science Engineering from Virginia Tech.

I have worked in the semiconductor industry since 1985.

I have been employed by Hewlett-Packard Company for six years and have been at my current position as an R&D Engineer for two years.

Exhibit A, entitled "Direct Tunneling Emitter Process Development and Improvement" and dated 1/12/2001 is a status report presented to Hewlett-Packard management that describes the differences observed between annealed and unannealed metal cluster emitters. The data contained within is believed to be a true and accurate copy of data collected during experiments performed on test devices at Hewlett-Packard facilities.

Exhibit B, entitled "Thick #1 SiC 50nm EFE051505_009 R6C2 (35um)," dated 2/21/2001 is a test report describing emitter test results of emitters using the invention. The data contained within the report is believed to be a true and accurate copy of data collected during experiments performed at Hewlett-Packard

facilities. The report lists the results of electrical testing on emission currents of the SiC emitters.

Exhibit C, entitled "Nano Holes in Thin Metal Layer – A Key for the Electron Emission for Flat Emitter Device" and undated is a Powerpoint slide presentation presented to Hewlett-Packard management. The data contained within the report is believed to be a true and accurate copy of data collected during experiments performed at Hewlett-Packard facilities. The report demonstrates the changes in the cathode layer due to the affects of annealing the metal cluster emitters.

Exhibit D, entitled "Emitter Energy Testing" and undated represents the test setup used to measure the diode and emission currents. This exhibit is presented to help the reader to better understand how the results listed in Exhibit B were obtained.

I further declare that all statements made herein of my own knowledge are true an that all statements made on information and belief are believed to be true; and that these statements were mad with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issuing thereon.

Signed:


Zhizhang Chen

Date: November 19, 2002

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To: Lori Tully, Paul Benning, James Smith, Tom Novet, David Schut, Bao Yeh, Mike Regan, Paul Harmon, Paul McClelland, David Pidwerbecki, John Bamber, Tim Myer, Jim Brug, Steve Naberhuis, Hueipei Kuo, Sity Lam, Henryk Birecki, Paul Cooperrider,
CC: JP Whitlock, Cathy Peltier, Clint Zlatnik, Tim Koch, Thomas Lindner, Laura king, and Jim McMahon

From: John Chen, Sriram Ramamoorthi, Mark Johnstone,
Brian Bolf, Todd Berdahl, Terry McMahon, David Neiman

Date: 1/12/2001

Direct tunneling emitter process development and improvement

Summary

Three major process changes have been made since the first cycle of learning on direct tunneling emitter. First, Pt dry etch process was developed to replace the oxide trench etch to resolve emitter isolation issue; Secondly, a dielectrics lift-off process was developed and process flow was redesigned so that emission layer was deposited after first layer metal etch to effectively prevent top to bottom electrode shorting; Third, an annealing process was implemented to improve device yield and emission test. The experiments showed that by using this improved process, the isolation between emitters and top to bottom electrode shorting became no issue, and annealing process improves device performance significantly. Comparing with non annealed process, annealed emitters make emission last longer and more repeatable, and device yield increases to 40 % from 12.5%.

Significant improvements were made, some of major challenges, however, are still ahead, such as low emission current density (~ 0.1 A/cm² is the current density measured, 1 A/cm² is the goal), emission flickering, and we also need to show focusing capability on MIS emitter device. These issues will be the main focus for our next move.

Process integration

Two cycles of learning on fabrication process of direct tunneling emitter were summarized in this report. The first cycle was served as process debug for unite process and whole process flow as well. The first cycle of direct tunneling process and structure is shown in Figure 1. There were two major issues we learn from the first cycle: 1. Emitter to emitter (or pad to pad) isolation issue; and 2. top to bottom electrode shorting. Failure analysis showed that the root cause of isolation failure between emitters is the results of combination of insufficient oxide trench and better than expected step coverage from Pt deposition. The top to bottom electrode shorting was caused by insufficient etch selectivity of Ta etch process, which is very difficult to achieve for the tunneling thin films we are using. Because of these issues, the pad to pad resistance was measured ~ 10 Ohms, and top to bottom electrode resistance is less than 100 Ohms.

Major process steps in first cycle

1. Define emission area by FOX
2. Emission layer deposition
3. Ta/Au (500 A/2000 A) deposition
4. Metal 1 photo patterning
5. Au wet etch
- 6 Ta dry etch
7. Trench photo
8. Oxide trench etch
9. Top thin metal deposition (50 – 100 A)

Exhibit A-10 of 6

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With Pt etch process the emitter isolation improved significantly. The emitter with Pt etch isolation was shown in Figure 3, where emitter area before and after the Pt etch isolation were shown. The test showed that this isolation is very effective. The pad to pad resistance increased from ~10 Ohms with oxide trench isolation to a typical value greater than 30 M-Ohms with Pt etch isolation. In most measurements, the resistance value is out of measurement range.

A dielectrics lift-off process was developed and process flow was redesigned so that emission layer was deposited after first layer metal etch to effectively prevent top to bottom electrode shorting. With this process flow change and the dielectric layer lift-off process, the very high selectivity requirement for metal etch is no longer needed. The top to bottom shorting was prevented effectively, and it become no issue.

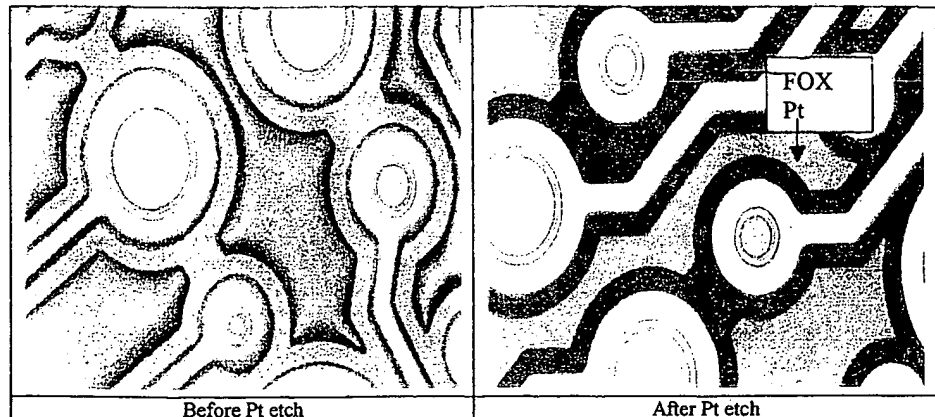


Figure 3 Pt etch isolation

Annealing Effects

Annealing experiments were done at two different conditions 400 C and 600 C, all with N2 purge and with 20 min duration. The annealing was done in a RTP system with no vacuum capability. The annealing conditions were shown in Figure 4 for both 400 C and 600 C anneal.

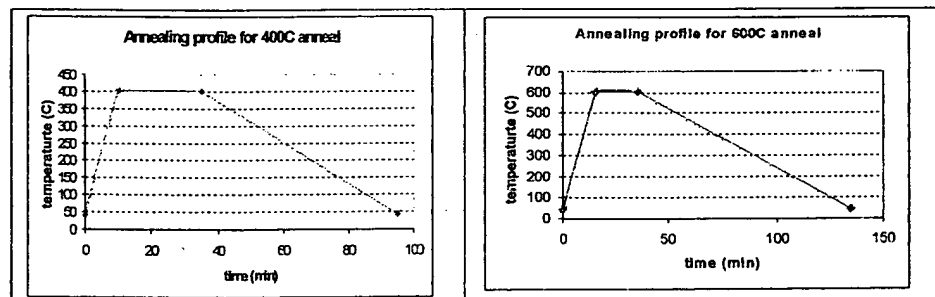


Figure 4 Annealing profile for 400 C and 600 C annealing.

A comparison of emission result between annealed and non-annealed emitter were shown in Table 1. More detailed emission result can be found from David Pidwerbecki's presentation (1/8/2001). Comparing with non annealed process, the annealed emitters make emission longer (last about minutes, instead of seconds from non annealed emitter), and most of all, the annealed emitters make repeatable emission test for the first time, and device yield increases to 40 % from 12.5%. In this set of experiments, the 400 C anneal gave a better emission results, as shown in Table 1.

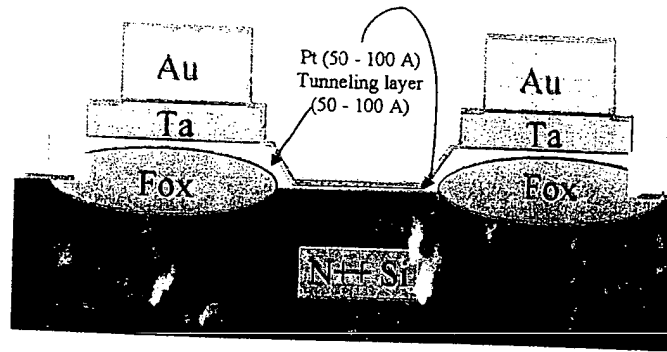


Figure 1. First generation of direct tunneling emitter design.

The second cycle of experiments were initiated to address the isolation and shorting issues. Three major changes were made. First, Pt dry etch process was developed to replace the oxide trench etch to resolve emitter isolation issue; Secondly, a dielectrics lift-off process was developed and process flow was redesigned so that emission layer was deposited after first layer metal etch to effectively prevent top to bottom electrode shorting; Third, an annealing process was implemented to improve device yield and emission test. The major process steps and structure were designed as shown in figure 2.

Improved process flow and major steps

1. Define emission area by FOX
2. Ta/Au (500 A/2000 A) deposition
3. Metal 1 photo patterning
4. Au wet etch
5. Ta dry etch
6. Tunneling layer dep./lift off
7. Top thin metal dep. (50 A - 100 A)
8. Trench photo
9. Thin metal etch (or lift-off)
10. Anneal

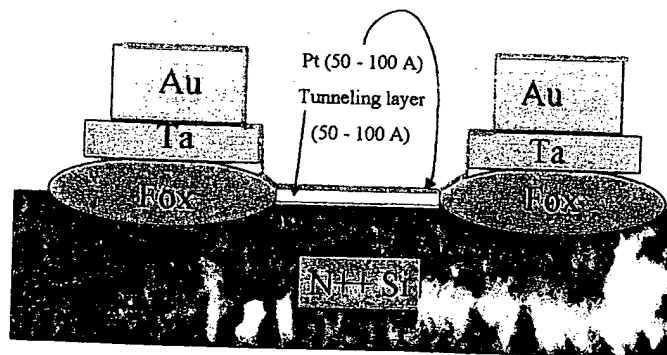


Figure 2 Improved structure to provide good isolation and prevent top to bottom electrode shorting.

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Table 1. Summary of emission results for different emission film and annealing conditions.

Emission material (thickness)	Wafer ID	# emitter tested	# emitter emitted	Yield (%)	Emission repeatable	Anneal
WSiN(50)	E1	8	1	12.5	No	No
WSiN(50)	C1	8	0	0		No
WSiN(100)	E3	40	4	10	No	No
WSiN(100)	C3	8	0	0		No
TiOx(50)	E5	32	0	0		No
TiOx(50)	C5	32	0	0		No
TiOx(100)	E6	8	1	12.5	No	No
TiOx(100)	C6	21	0	0		No
WSiN(50)	E1-600C	35	10	29	Yes	Yes-600C
TiOx(100)	E6-600C	35	7	20	Yes	Yes-600C
TiOx(100)	E6-400C	35	14	40	Yes	Yes-400C

Note: E-wafer edge; C-wafer center.

Some analyses were done to understand the effect of annealing. Figure 4 showed the I - V characteristics for annealed and non annealed emitter, respectively. It showed that at a fixed voltage, the tunneling current for the annealed emitter is about 3 time higher than non annealed emitter. If we took the slope of voltage versus current, we found that the device series resistance for annealed emitter is 3 times lower than non annealed emitter. Therefore, it suggests that the effective electric field to enhance tunneling is higher for annealed emitter than for non annealed emitter at given voltage.

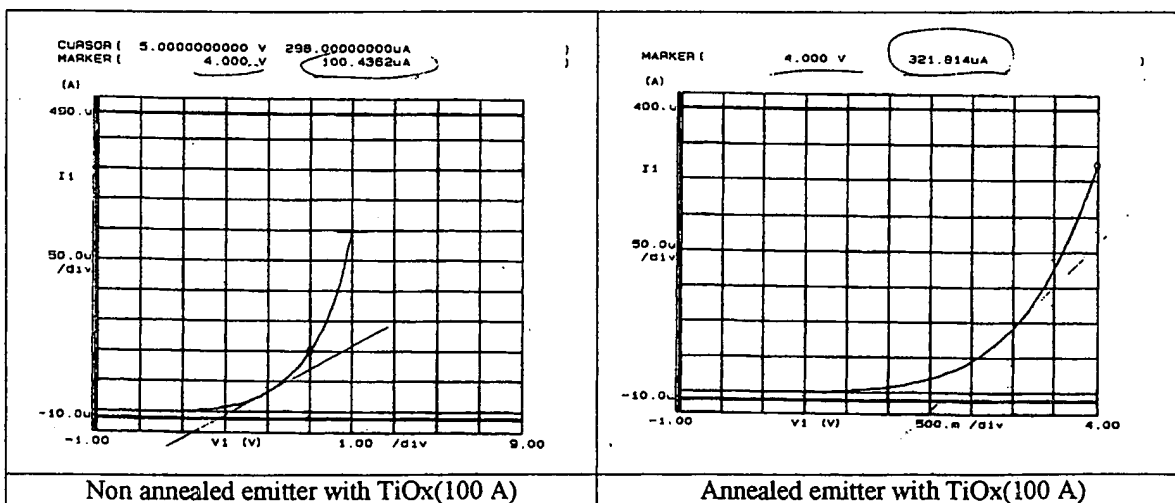


Figure 4 I-V characteristics for annealed and non annealed emitters, respectively

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Many researchers have point out the correlation between electron emission and light emission. Some of useful information can be found from the light emission measurements. The light emission measurements were done for annealed and non annealed emitter, respectively. The results are shown in Figure 5. It can be seen that a relative uniform light emission pattern produced by annealed emitter comparing to non annealed emitter. Also it should be pointed out that in order to clearly show the light emission from non annealed emitter high voltage is needed. For example, the light emission can be measured clearly with 4 V for annealed emitter, while 5V had to be applied to the non annealed emitter, as shown in Figure 5. Again, it showed that the effective field on annealed emitter is higher than non annealed emitter. Figure 5 also indicated a better interface, less hot spots for annealed emitter comparing non annealed emitter. From Figure 4 and 5, it may conclude that with annealing, device series resistance is reduced and effective field is increased, also relative uniform interface is produced.

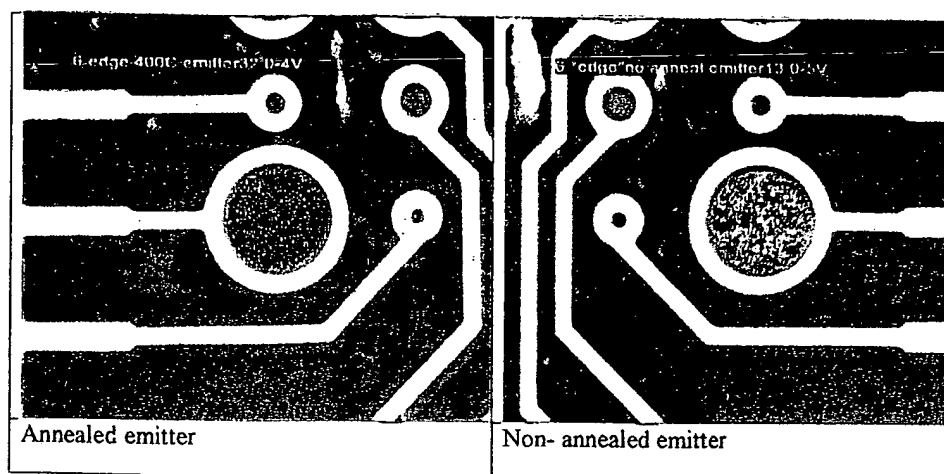


Figure 4. Annealing effect on light emission pattern

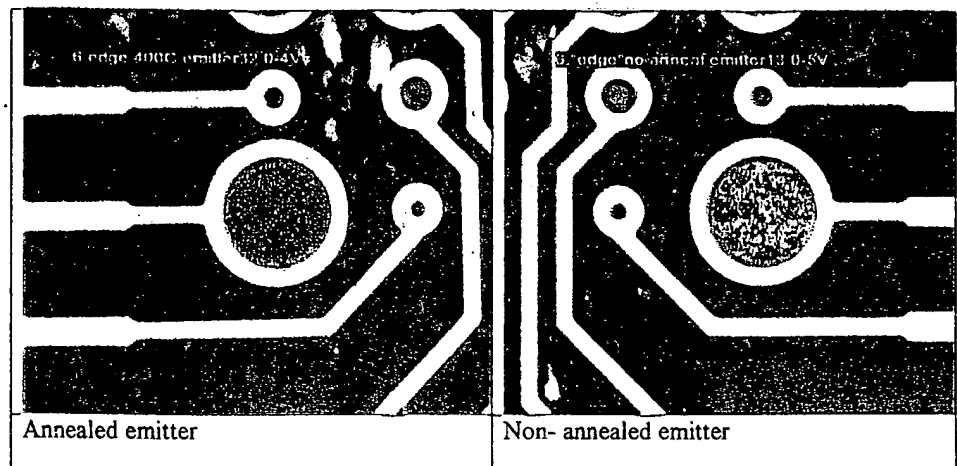
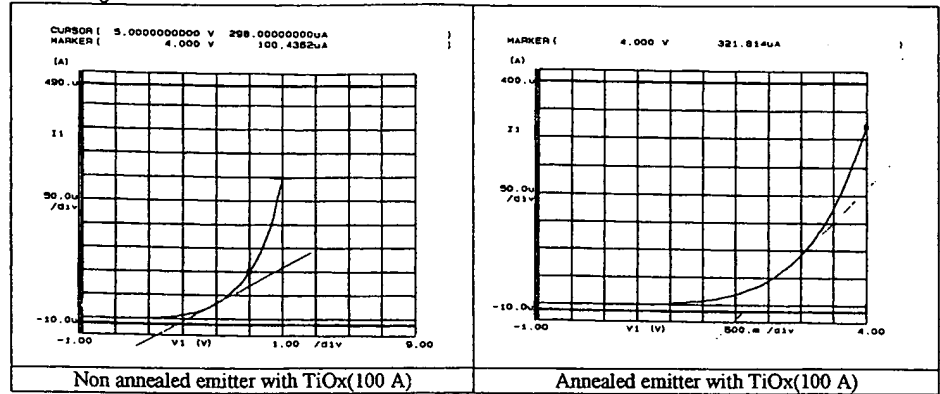
Path forward

Some of major challenges will be addressed, such as low emission current density ($\sim 0.1 \text{ A/cm}^2$ is the current density measured, 1 A/cm^2 is the goal), emission flickering, and focusing capability. The optimization of emission layer thickness (thicker direct tunneling film in the range of $100 - 250 \text{ \AA}$ is planned), annealing condition (forming gas effect), and Pt thickness control will target on low emission current and device yield improvement. Device structure and emission material modification may be needed to address the flickering issue. And two metal parts process development will address the emitter focusing capability.

Acknowledgement

This project could not happen without support from ORCA program, especially, the strong support and inspiration from Lori Tully and Mike Regan. Special thanks to Tom Novet for his great effort and ground work in the early MIS emitter process development. Thanks to Paul Benning for many useful discussions. Thanks to David Pidwerbecki and David Schut for the emission test and communicating the results. And of course, none of this would happen without the continued managerial support of JP Whitlock, Cathy Peltier, and Clint Zlatnik from B2 fab operation.

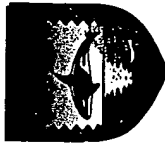
Annealing Effects





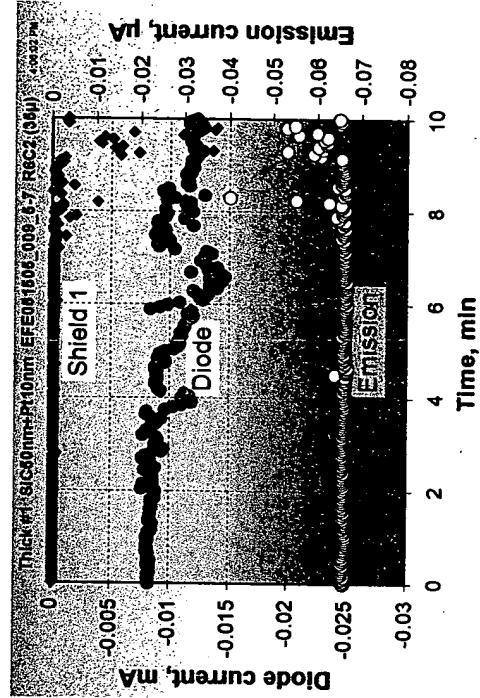
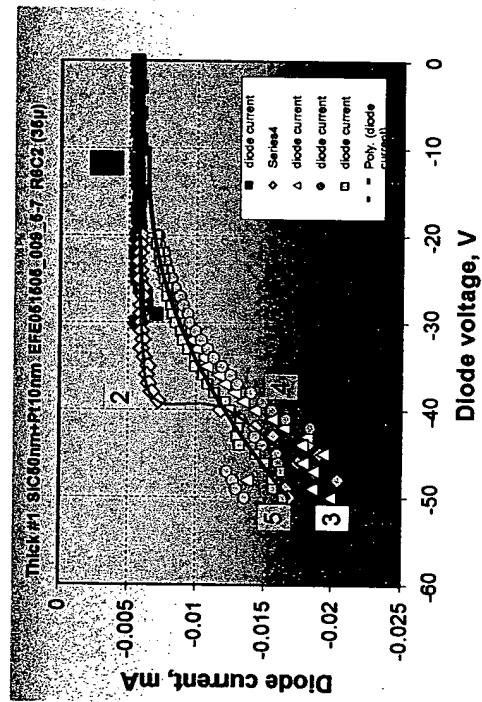
21 February 2001

Thick #1 SiC 50nm EFE051505_009 R6C2(35μm)



Orca.cv

- First run



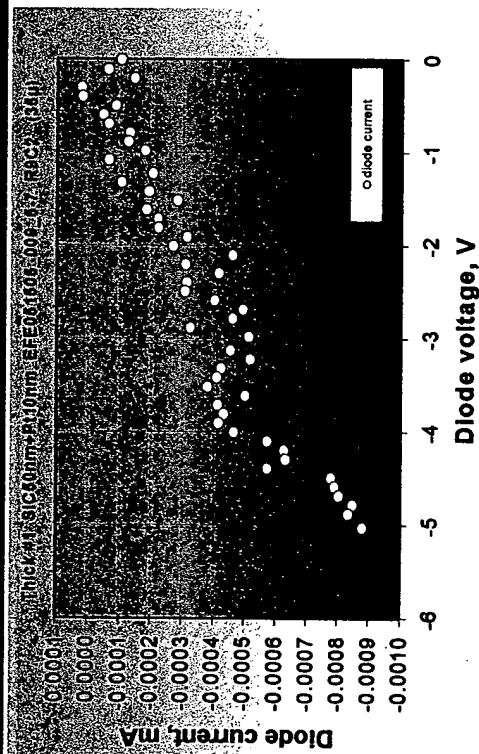


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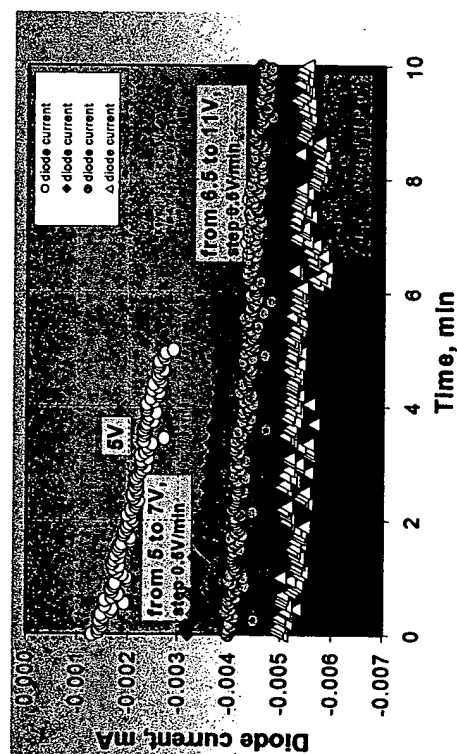
Thick #1 SiC 50nm EFFE051505_009_5-7 R9C2(35μm)



Orca.cv



- Very low diode current at 5...2 V - 1...6 nA
- Some sort of conditioning ?
- Or just DVM drift?



- increase voltage
- and increase time ?
- Increase temperature
- Decrease thickness

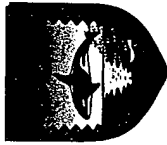
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Alex Goyvadinov

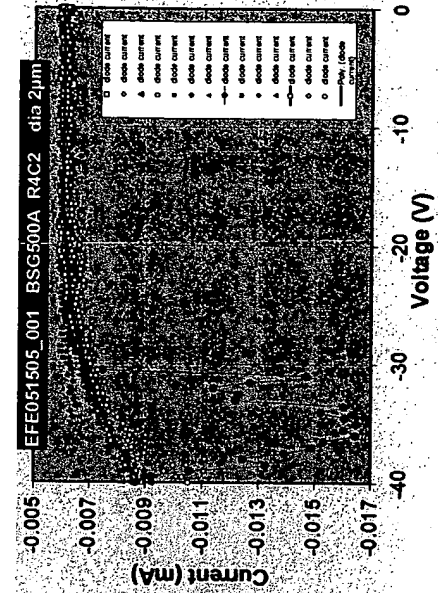
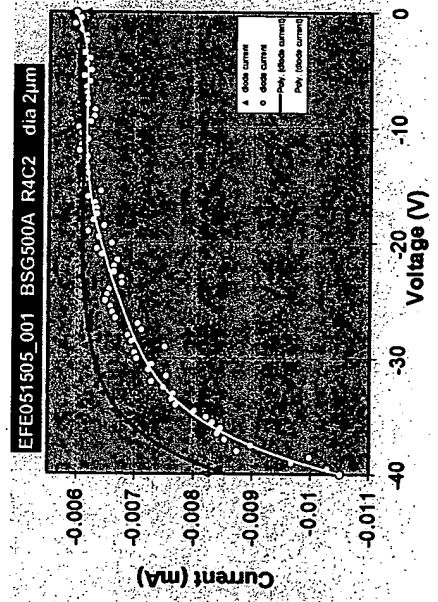
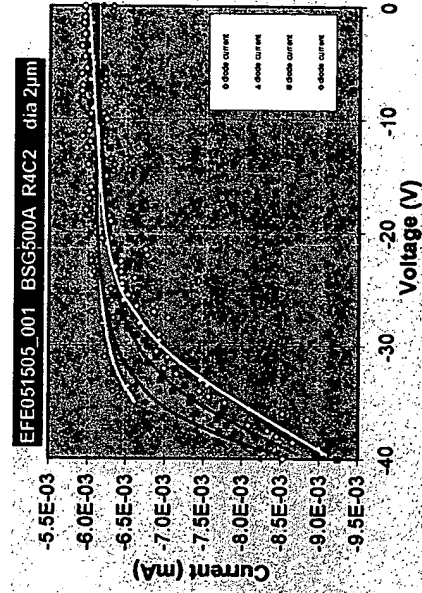
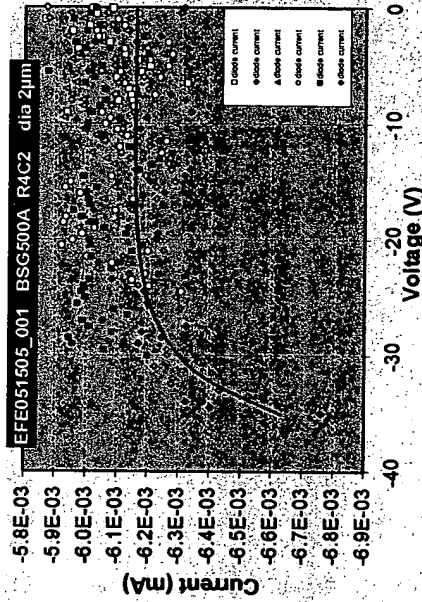


21 February 2001

Thick #1 BSG 50nm EFE051505_001 R4C2(2μm)



Orca.cy



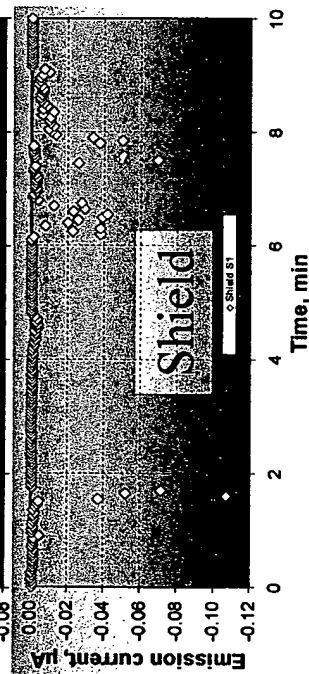
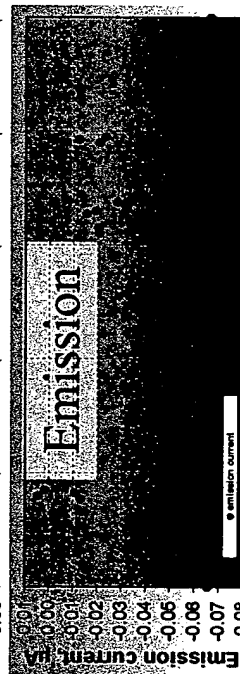
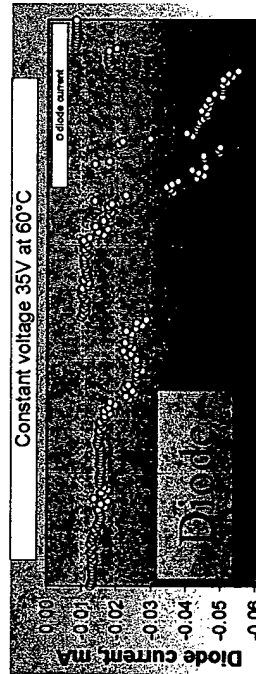


21 February 2001

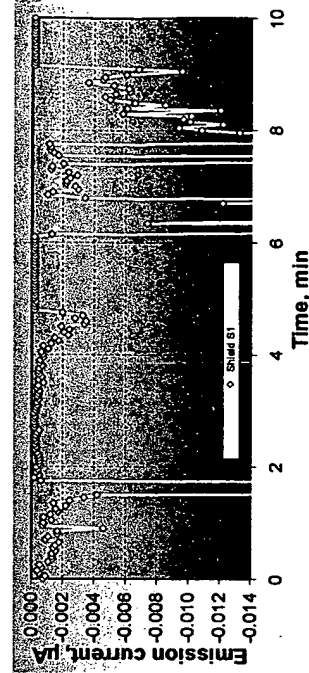
Thick #1 SiC 50nm EFE051505_009 R6C2(35 μ m)-continue



Orca.cv



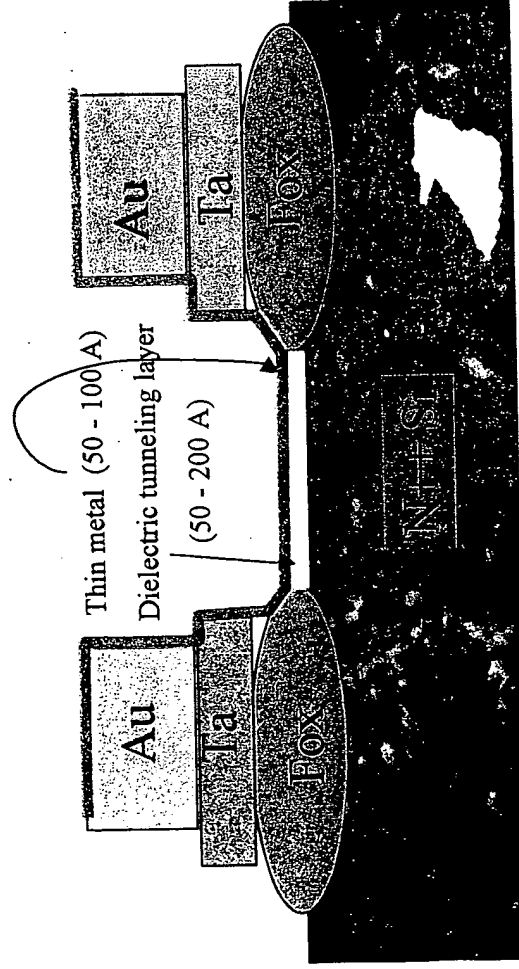
- Second run at ~60°C
- ~120 nA peak emission
- Average emission - 5nA



Nano holes in thin metal layer- A key for the electron emission for flat emitter device

1. Nano holes provide electron emission sites which is a key for electron emission.
2. Nano holes may improve the emission reliability of emitters.
3. Nano holes reduce spiking and improves emission stability.
4. Nano holes can be produced in thin metal layer, such as Pt and Ta/AU by using appropriate annealing process.
5. Annealing ambient and temperature are the two critical process parameters to produce and control the nano holes. In this invention, we found that the temperature is in a range of 400C – 650 C, and nitrogen ambient is the key to generate the nano holes, while oxygen and Argon are not effective.

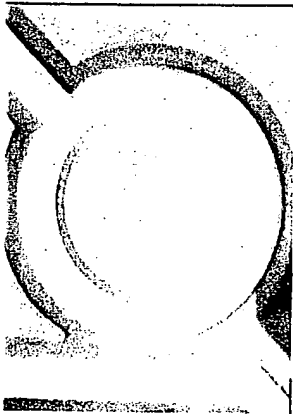
Flat emitter structure



Second generation process

1. define emission area by FOX
2. Ta/Au Deposition
3. Metal 1 photo patterning
4. Au wet etch
- 5 Ta dry etch
6. Tunneling layer dep /lift off
7. Top thin metal dep Pt or Ta/Au.
8. trench photo
9. thin metal etch

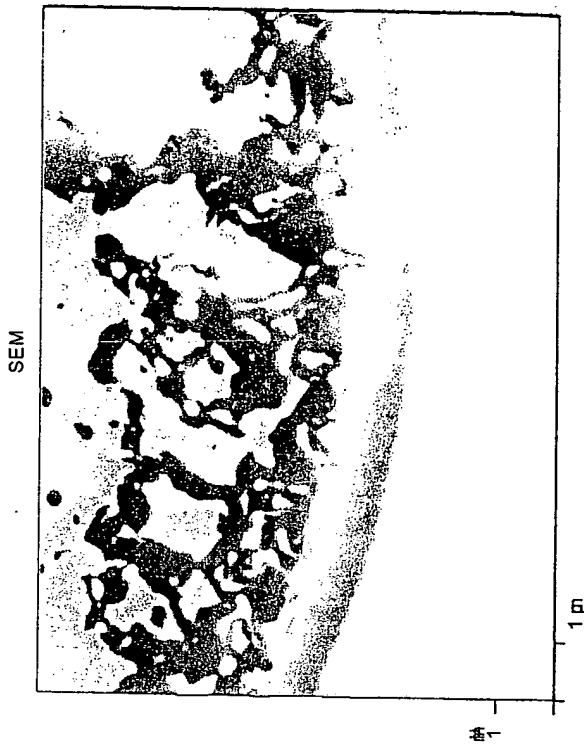
Electrical breakdown Damage on thin metal layer

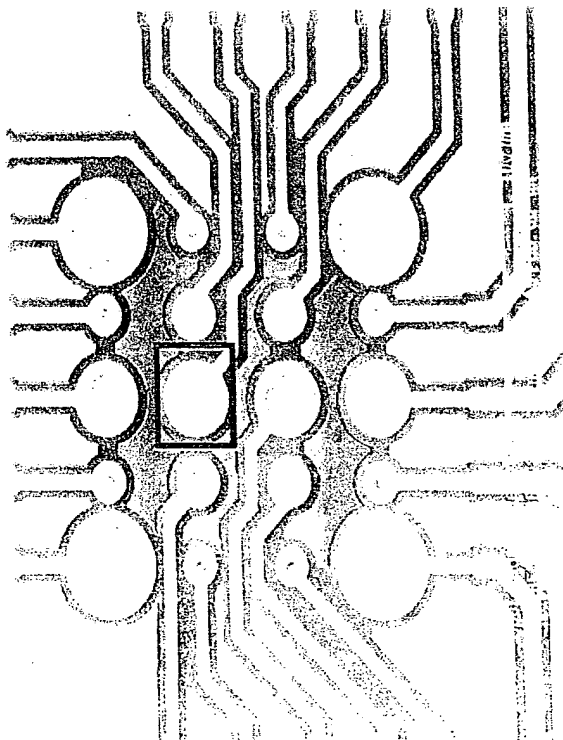


As deposit



Early breakdown damage



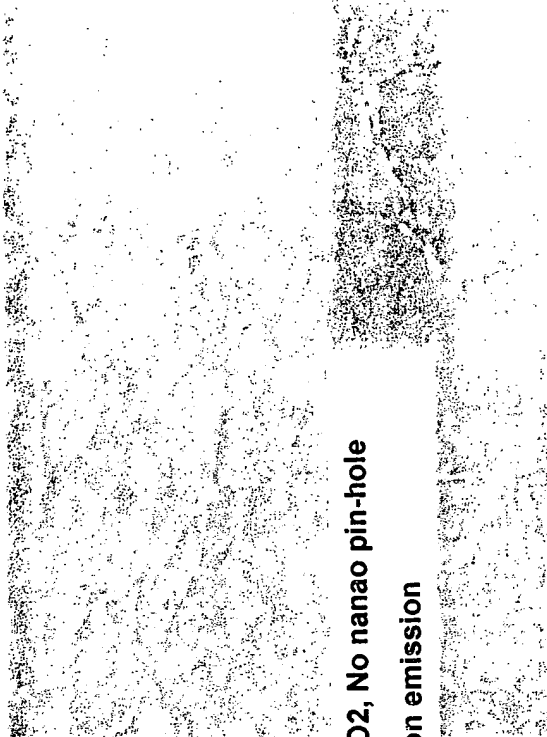


Nano hole development in thin metal

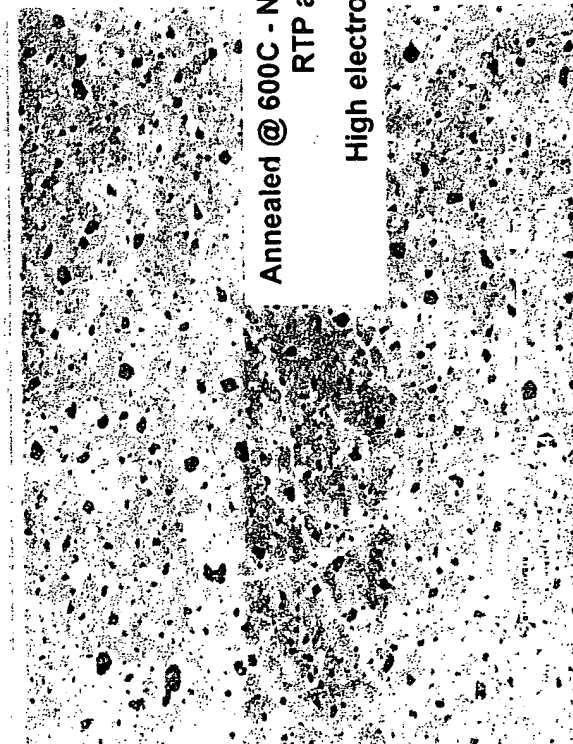
As deposited thin Pt film with thickness $\sim 7\text{ nm}$
No nano holes structure in this film.
No electron emission.

Annealed @ 450 - O₂, No nano hole
No electron emission

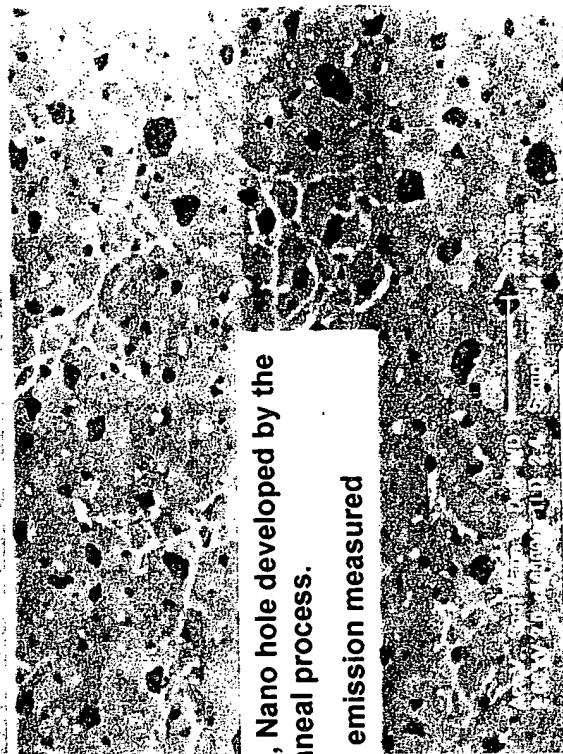
Annealed @ - 450 - N₂, nano hole starts grow
and electron emission detected

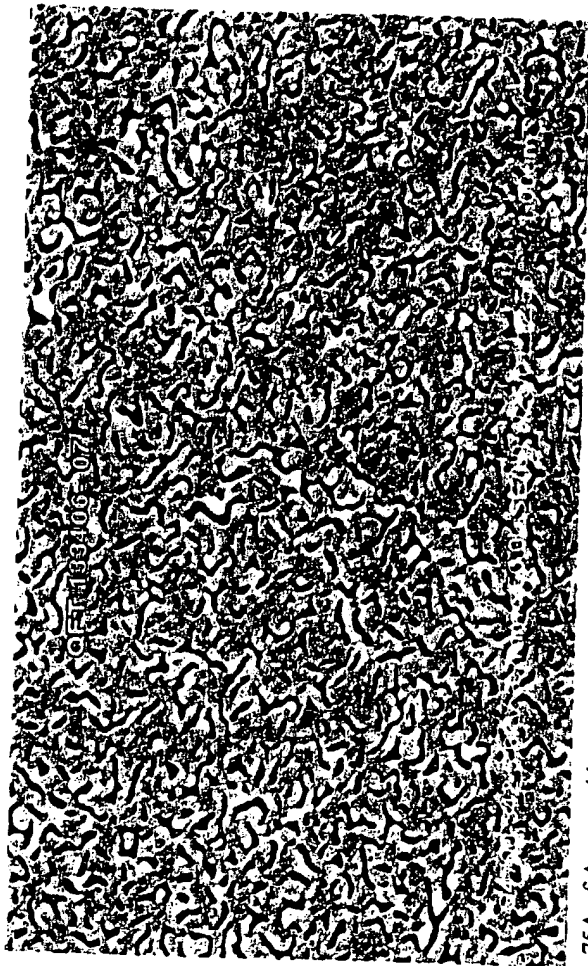


Annealed @ 600C - O₂, No nano pin-hole
No electron emission



Annealed @ 600C - N₂, Nano hole developed by the
RTP anneal process.
High electron emission measured





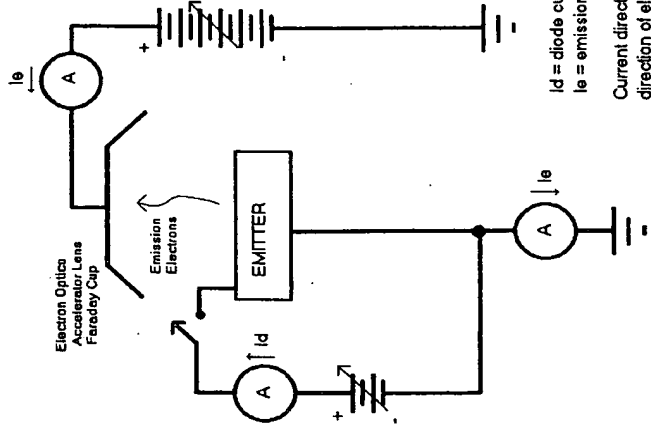
75A of Au on oxide

600x N₂

Emitter Energy Testing

Chip Testers 2 and 4 are versatile, automated emission testers capable of accurately measuring emission and diode currents from Porous Silicon, MIS, and Spindt Tip emitters. The testers are a hybrid of commercially available instrumentation and custom instrumentation.

Patent Application 10007763
Serial No. 09/846,047



Outputs (Voltages)	Range	Precision
Diode Voltage	0 to 100 Volts	1%
Focusing Voltage	-100 to 100 V	1%
Accelerator Lens	0 to 2000 Volts	1%
Faraday Cup Voltage	0 to 2000 Volts	1%
Inputs (Currents)		
Id (Diode Current)	-4 to 40 mA	5 uA
Ie (Emission Current)	-8 to +8 uA	1 nA
I _L (Accelerator Lens Current)	-8 to +8 uA	3 nA
I _F (Faraday Cup Current)	-8 to +8 uA	3 nA

